10 - 17 - 00

A

Practitioner's Docket No. **GR 97 P 1049 D**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

DIVISIONAL APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventors:

BERNHARD SCHÄTZLER et al.

For (title):

Electronic Component with an Integrated Circuit Mounted on an Island of a Lead Frame

1. Type of Application

This new application is for a

[x] Divisional.

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

[x] The new application being transmitted claims the benefit of prior U.S. application. Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for Filing Date under 37 C.F.R. 1.53(b)

__14__ Pages of Specification
__2__ Pages of Claims
__1__ Sheet of Drawing
[x] Formal
[ ] Informal

B. Other Papers Enclosed

__1__ Page of Abstract
____ Other

4. Additional Papers Enclosed

[ ] Preliminary Amendment
[x] Information Disclosure Statement (37 C.F.R. 1.98)
[x] Form PTO-1449 (PTO/SB/08A and 08B)
[ ] Citations
[ ] Declaration of Biological Deposit
[ ] Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
[ ] Authorization of Attorney(s) to Accept and Follow Instructions from Representative
[ ] Special Comments
[ ] Other

5. Declaration or Oath

[x] Enclosed
Executed by
[x] inventors.

6. Inventorship Statement

The inventorship for all the claims in this application are:

[x] The same.

7. Language

[x] English

8. Assignment

[x] An assignment of the invention to Siemens Aktiengesellschaft

[x] will follow.

9. Certified Copy

Certified copies of applications: None

11. Fee Payment Being Made at This Time

[x] Enclosed

[x]	Filing fee	$710.00
	Total Fees Enclosed	$710.00

12. Method of Payment of Fees

[x] Check in the amount of $710.00.

15. Authorization to Charge Additional Fees

[x] The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 12-1099.

[x] 37 C.F.R. 1.16(a), (f) or (g) (filing fees)

[x] 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)

[x] 37 C.F.R. 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

[x] 37 CFR 1.17(a)(1)-(5) (extension fees pursuant to § 1.136(a).

[x] 37 C.F.R. 1.17 (application processing fees)

[ ] 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

16. Instructions as to Overpayment

[x] Credit Account No. 12-1099.

[ ] Refund

SIGNATURE OF PRACTITIONER

LAURENCE A. GREENBERG
REG. NO. 29,308

P.O. Box 2480, Hollywood, FL 33022
P.O. Address

Tel. No.: (954) 925-1100
Fax No.: (954) 925-1101

/bb

"Express Mail" mailing label number EL608558998US
Date of Deposit: October 16, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

MICHAEL J. BURNS

[x] **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

[x] Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added 1

[x] Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added 2

[ ] Plus added pages deleting names of inventor(s) named on prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added _____

[ ] Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

[ ] **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

[ ] This transmittal ends with this page.

ADDED PAGE FOR SPECIAL COMMENTS FOR NEW APPLICATION TRANSMITTAL

This is a division of U.S. application No. 09/359,178, filed July 22, 1999 which was a continuation of copending International Application No. PCT/DE97/00105, filed January 22, 1997, which designated the United States.

GR 97 P 1049 D

ELECTRONIC COMPONENT WITH AN INTEGRATED CIRCUIT MOUNTED ON AN ISLAND OF A LEAD FRAME

Cross-Reference to Related Application:

This is a division of U.S. application No. 09/359,178, filed July 22, 1999 which was a continuation of copending International Application No. PCT/DE97/00105, filed January 22, 1997, which designated the United States.

Background of the Invention:

Field of the Invention:

The invention relates to an electronic component, in particular to thin QFPs, in which a standardized lead frame and an integrated circuit are used and embedded in a casting or molding compound.

Surface mounted electronic components, also called SMD components, are usually embedded in a housing made of a plastic molding compound, from which electronic terminals are led out. Depending on the number of terminals required, these housings correspond to a standard having defined dimensions to enable standardized production and automatic component-mounting of circuit boards. The dimensions of these housings are defined in German and International

Standards. The lead frames, which are used for embedding the electrical terminals in an exactly positioned manner, are likewise standardized. An island is provided in the center of a lead frame and an integrated circuit is fixed on the island. A lead frame and an integrated circuit are then encapsulated together by molding them in a housing made of a molding compound. Stresses occur on account of the different expansion coefficients of the iron/nickel alloy usually used for the lead frame, of the silicon chip forming the integrated circuit, and of the molding compound of the housing. The occurrence of reaction shrinkage of the molding compound creates stresses as well. Consequently, diagonal housing warpage of up to 100 µm occurs particularly in the case of large flat housings (thin QFPs, also called TQFPs).

Attempts are made to prevent this housing flexure or warpage by using special island structures. In these cases, holes or slots are made in the islands, which are arranged centrally in the lead frames. Alternatively, the islands are undercut or furrows are etched into the islands. The use of copper lead frames has also already been attempted in order to minimize the housing warpage. However, all of these solutions require either new or changed mounting processes, or they can be implemented only with etched lead frames, not with stamped lead frames, or they lead to a reduction in the rigidity of the external terminals.

German published, non-prosecuted Patent Application DE 36 35 375 A1 discloses the use of a standardized lead frame. In this case, in order to adapt the carrier island to the semiconductor component, a corresponding carrier island is fixed on the central part of the frame.

In order to avoid flexure of a potted element, published European Patent Application EP 0 261 324 A1 discloses arranging the lead frame such that it is centered in height terms in the potting mold in order to ensure that the same amount of plastic reaches above and below the integrated circuit.

Patent Abstracts of Japan Publication No. 60189956 discloses adapting a lead frame configuration having a chip island on which a semiconductor chip is to be disposed to the size of the chip in such a way that the chip island is reduced to the size of the semiconductor chip by removing an edge.

U.S. Patent No. 4,258,381 describes a lead frame configuration which is intended to be suitable for accommodating different chip sizes. The dimensions to be adhered to for the chip island are specified in this case.

Summary of the Invention:

It is accordingly an object of the invention to provide an electronic component, in particular to thin QFPs, in which a standardized lead frame and an integrated circuit are used and embedded in a casting or molding compound, which overcomes the above-mentioned disadvantages of the heretofore known methods and devices of this type, and which minimize flexure of the housing in a structurally simple manner.

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for producing an electronic component, which includes the following steps: Producing a standardized lead frame having a predetermined number of leads that can be used with any one of a plurality of integrated circuits having different base areas. Producing the standardized lead frame with a central island having a predetermined maximum base area for supporting any one of the plurality of integrated circuits. Selecting one of the plurality of integrated circuits. Reducing the base area of the island, in accordance with a base area of the selected integrated circuit to obtain a ratio between the base area of the selected integrated circuit and the base area of the island from 0.7 to 0.9. Fixing the selected integrated circuit on the island, and embedding the selected integrated circuit and the island in a casting or molding compound so that a unit formed by the

selected integrated circuit and the island is substantially vertically centered within the casting or molding compound. An overhang of the island beyond the base area of the integrated circuit, which would result in asymmetry in the distribution of the molding compound, is avoided in this case to the greatest possible extent. What is achieved by this construction is that during the occurrence of reaction shrinkage of the molding compound, at the periphery of the integrated circuit, between the edge thereof and the island edge, stresses which lead to warpage of the housing do not occur. The adaptation of the island expediently takes place after the production of the standard lead frames, because then a completely standardized lead frame can be used. Alternatively, the process for adapting the size of the island may be integrated in the actual process for producing the lead frame. In that case, however, it is necessary to produce different lead frames with island sizes that are adapted to the respective size of the integrated circuit. The tools for producing the lead frame are constructed modularly in order to enable the island size to be adapted in a simple manner.

In accordance with an added feature of the invention, the provided method includes performing the steps of producing the standardized lead frame using a stamping process. The lead frame is preferably stamped with the island integrally

formed in it, in order to bring the island to the desired size. As an alternative, it is also possible to process the lead frame and the island using etching processes.

In accordance with an additional feature of the invention, the selected integrated circuit is preferably fixed on the island by bonding using a silver conductive adhesive.

In accordance with another feature of the invention, the provided method includes using an adhesive to perform the step of fixing the selected integrated circuit on the island, and monitoring the adhesive emerging from between the selected integrated circuit and the island to determine the quality of the fixation between the selected integrated circuit and the island. The base area of the island is usually reduced to a size that is still slightly larger than the base area of the integrated circuit so that the emerging adhesive can flow onto the edges of the island or the island overhang. A hollow groove is formed in the region of the island overhang and can readily be monitored visually.

With the objects of the invention in view, there is additionally provided an electronic component that includes a housing made of a casting or a molding compound, an integrated circuit having a base area, and a lead frame having a central island with a base area supporting the

integrated circuit. The ratio between the base area of the integrated circuit and the base area of the island is from 0.7 to 0.9 for avoiding flexure of the housing. The integrated circuit and the island are embedded in the housing so that a thickness of a housing region above the integrated circuit is substantially equal to a thickness of a housing region below the island. This electronic component is distinguished by the fact that the island terminates essentially flush with the integrated circuit, and that the distance between the top side of the housing and the top side of the integrated circuit corresponds to the distance between the underside of the housing and the underside of the island. If the island is larger than the integrated circuit that is fixed on it, then the result is a different molding compound thickness between the top side of the island and the top side of the housing and the underside of the island and the underside of the housing, in the region of the island overhang. This difference in thickness, in interaction with the rigid lead frame made of a special metal alloy, causes stresses in the housing which result in the warpage of the housing. Given otherwise identical materials, manufacturing equipment, processes and process parameters, the ratio of the base area of the integrated circuit to the base area of the island, alone, determines the degree of warpage of the housing. The stresses between the integrated circuit, lead frame, and molding compound are balanced by adapting the base

area of the island to the respective base area of the integrated circuit in such a way that the warpage of the housing is reduced or eliminated, depending on the ratio of the areas to one another. In order to attain particularly good minimization of the warpage of the housing, the island can be constructed so that it terminates flush with the placed integrated circuit. In that case, the island and the integrated circuit therefore have exactly the same size or base areas. As a result, the molding compound thickness between the top side of the integrated circuit and the top side or edge of the housing and the underside of the island and the bottom side or edge of the housing are identical at all points in the housing and the stresses compensate for one another. The bimetal effect resulting from the different expansion coefficients is avoided due to the symmetrical construction.

In accordance with an added mode of the invention, the electronic component includes an adhesive, bonding the integrated circuit to the island, and a hollow groove that is formed on the integrated circuit by an amount of adhesive that has emerged from between the integrated circuit and the island. Because the base area of the island has been constructed somewhat larger than the integrated circuit, the emerging adhesive forms a hollow groove on the overhanging edge of the island. The formation of this groove makes it

possible to monitor whether or not the integrated circuit is correctly bonded on the island. It is particularly expedient in this case to construct the island in such a way that the ratio of the base area of the integrated circuit to the base area of the island is less than 0.9 : 1.0.

In accordance with an additional mode of the invention, the base area of the island is constructed as a continuous, unpatterned area. This ensures that the thickness of the molding compound above and below the integrated circuit and the island is identical. In addition, the prior-art patterning and special structures of the island are obviated.

In accordance with another mode of the invention, the lead frame includes leads that are routed up to the island. This is advantageous particularly in the case of very small integrated circuits, in which an excessively large distance between the leads and the island would be produced and problems might arise in the course of further contact-making.

In accordance with a further mode of the invention, the lead frame includes leads that are vertically centered within the housing, and the island is vertically lowered with respect to the leads.

In accordance with a concomitant mode of the invention, an electronic component is provided that includes a housing made of casting or molding compound, an integrated circuit having a base area, and a lead frame having an island with a base area supporting the integrated circuit. The base area of the island is greater than the base area of the integrated circuit for avoiding flexure of the housing. The integrated circuit and the island are embedded in the housing so that a thickness of a housing region above the integrated circuit is substantially equal to a thickness of a housing region below the island.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied as an electronic component with an integrated circuit mounted on an island of a lead frame and a method for producing the electronic component, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages

thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic lateral-sectional view of a component according to the invention with a large integrated circuit;

Fig. 2 is a lateral-sectional view through a component according to the invention with a small integrated circuit; and

Fig. 3 is a lateral-sectional view through a component according to the invention with a small integrated circuit and an island that terminates flush with the integrated circuit.

Description of the Preferred Embodiments:

Referring now to the features of the drawings in detail and first , particularly, to Fig. 1 thereof, there is seen a cross section through an electronic component with a lead frame 2, that includes leads 3 and an island 4. An integrated circuit 1 is fixed on the island 4, and the lead frame 2 and the integrated circuit 1 are then embedded in a housing 6 made of molding compound. The integrated circuit 1

and the island 4 are vertically disposed to produce housing regions 7 and 8 respectively having a thickness a and b, that are identical. The size of the island 4 has been adapted, in accordance with the invention, to the base area of the integrated circuit 1, with the result that these essentially correspond. The island 4 is larger than the base area of the integrated circuit 1 merely by a small overhang, with the result that the adhesive used to fix the integrated circuit 1 on the island 4 can escape and form a hollow groove 5 on the overhang. This hollow groove 5 forms a suitable monitoring parameter for monitoring optimum bonding of the integrated circuit 1 to the island 4. The whole lead frame 2 is vertically disposed so that the leads 3 are likewise vertically centered in the housing 6. Therefore, housing regions having the same thickness, which are designated by reference symbol c in Fig. 1, extend above and below the leads 3. The island 4 is lowered relative to the leads 3, in accordance with the height of the integrated circuit 1 so that the combined height of the integrated circuit 1 and the island 4 will be vertically centered within the housing 6. This height adaptation is to be taken into account during the production of the lead frame 2 and the connections between the leads 3 and the island 4.

Fig. 2 illustrates an electronic component according to the invention with a small integrated circuit 11. For this

purpose, the island 14 is adapted in accordance with the smaller integrated circuit 11 and is accordingly constructed to be smaller. A suitable ratio of the base area of the integrated circuit 11 to the base area of the island 14 lies between 0.7 and 0.9, as can be gathered from Table I.

In experiments with various TQFP 20 x 20 x 1.4 mm housings, alloy-42 lead frame and Aratronic 2188 molding compound, the following relationships were determined.

TABLE I

Island size in mm x mm	Chip area/island area ratio (average	Housing warpage diagonal value)
13.8 x 13.8	0.7	< 80µm
13.8 x 13.8	0.8	< 60µm
13.8 x 13.8	0.9	< 20µm
11.6 x 11.6	0.6	> 70µm
9.4 x 9.4	0.6	> 80µm
9.4 x 9.4	0.9	< 30µm

Within the lead frame 2, the island 14 is lowered relative to the leads 3 so that housing regions having the same thickness c are produced both above and below the leads 3, and so that housing region 7 having the thickness a and housing region 8 having the thickness b substantially equal to thickness a are respectively produced above and below the combination of the integrated circuit 11 and the island 14. In this exemplary

embodiment, a small overhang of the island 14, at which stresses occur due to the reaction shrinkage of the molding compound, is accepted so that a hollow groove 5 can be produced on the island overhang. The hollow groove serves as an important monitoring parameter during production.

Another embodiment of the invention is shown in Fig. 3, which illustrates a small integrated circuit 11 with an island 24 that terminates flush with the integrated circuit 11. Overhanging island regions at which stresses could occur due to the reaction shrinkage of the molding compound are not present at all in this embodiment.

The figures merely illustrate integrated circuits 1 and 11 having two different sizes. It goes without saying, however, that a whole group of integrated circuits of different sizes can be used with a standardized housing 6. The size of the island 4 is adapted in accordance with the size of the base area of a selected integrated circuit, in such a way that the standard lead frame 2 is processed further in accordance with the invention and can be used for a whole group of different integrated circuits, without warpage of the housing 6 occurring. The housings 6 described above are large thin square housings, so-called TQFPs, having 176 leads, for example, that are led out from the square housing on all four sides.

We claim:

1. An electronic component, comprising:

a housing made of a casting or a molding compound;

an integrated circuit having a base area; and

a lead frame having an island with a base area supporting said integrated circuit, a ratio between the base area of said integrated circuit and the base area of said island being from 0.7 to 0.9 for avoiding flexure of said housing;

said integrated circuit and said island embedded in said housing so that a thickness of a housing region above said integrated circuit is substantially equal to a thickness of a housing region below said island.

2. The electronic component according to claim 1, including an adhesive bonding said integrated circuit to said island, and a hollow groove formed on said integrated circuit by an amount of adhesive that has emerged from between said integrated circuit and said island.

3. The electronic component according to claim 1, wherein the base area of said island is a continuous, unpatterned area.

4. The electronic component according to claim 1, wherein said lead frame includes leads that are routed to said island.

5. The electronic component according to claim 1, wherein said lead frame includes leads that are vertically centered within said housing, and said island is vertically lowered with respect to said leads.

6. An electronic component, comprising:

a housing made of casting or molding compound;

an integrated circuit having a base area; and

a lead frame having an island with a base area supporting said integrated circuit, the base area of said island being greater than the base area of said integrated circuit for avoiding flexure of said housing;

said integrated circuit and said island embedded in said housing so that a thickness of a housing region above said integrated circuit is substantially equal to a thickness of a housing region below said island.

Abstract of the Disclosure:

A method for producing an electronic component, includes producing a standardized lead frame having a predetermined number of leads that can be used with any one of a plurality of integrated circuits having different base areas. The standardized lead frame is produced with an island having a predetermined maximum base area for supporting any one of the plurality of integrated circuits. One of the plurality of integrated circuits is selected. The base area of the island is reduced, in accordance with a base area of the selected integrated circuit, to obtain a ratio between the base area of the selected integrated circuit and the base area of the island of from 0.7 to 0.9. The selected integrated circuit is fixed on the island, and the selected integrated circuit and the island are embedded in a casting or molding compound so that a unit formed by the selected integrated circuit and the island is substantially vertically centered within the casting or molding compound. An electronic component produced by the method is also provided in which flexure of the housing is reduced.

MPW/bb

FIG 1

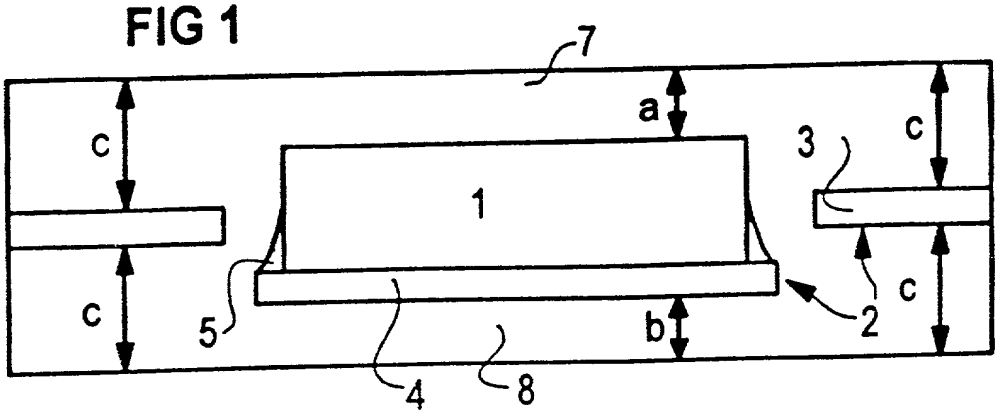


FIG 2

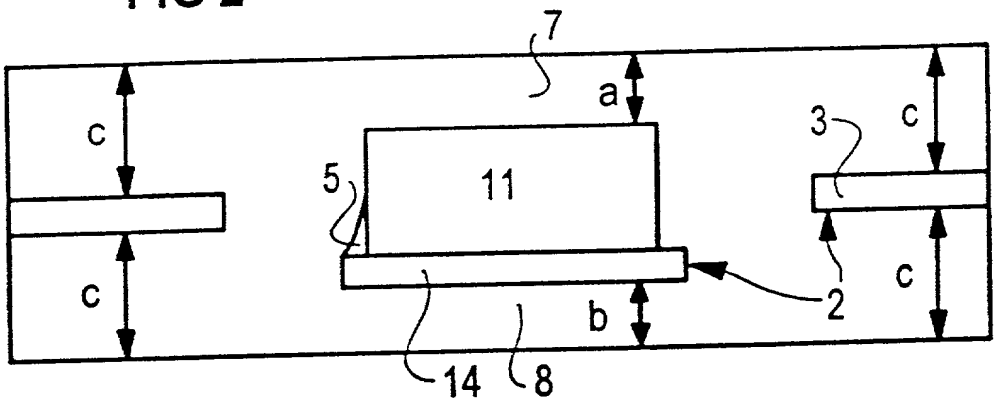
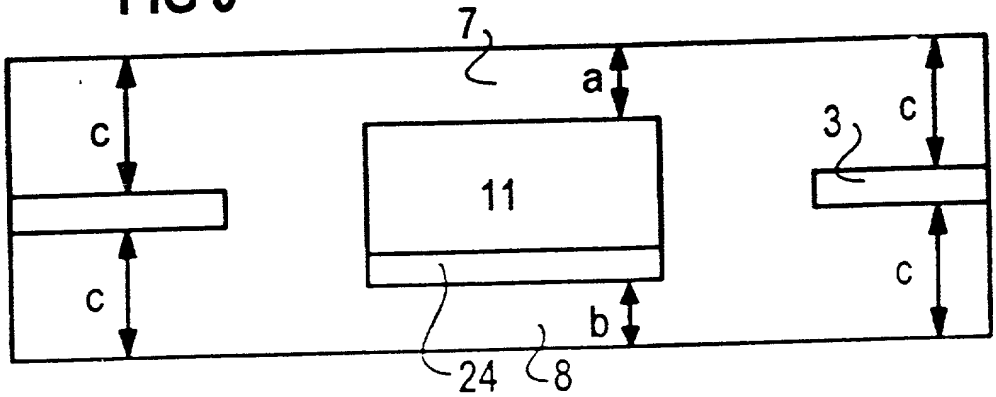


FIG 3



Docket No.: GR 97 P 1049

COMBINED DECLARATION AND POWER OF ATTORNEY IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRONIC COMPONENT WITH AN INTEGRATED CIRCUIT MOUNTED ON AN ISLAND OF A LEAD FRAME AND A METHOD FOR PRODUCING THE ELECTRONIC COMPONENT

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

International Application No. PCT/DE97/00105, filed January 22, 1997, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

HERBERT L. LERNER (Reg.No.20,435)
LAURENCE A. GREENBERG (Reg.No.29,308)
WERNER H. STEMER (Reg.No.34,956)
RALPH E. LOCHER (Reg.No. 41,947)

Address all correspondence and telephone calls to:

LERNER AND GREENBERG, P.A.
POST OFFICE BOX 2480
HOLLYWOOD, FLORIDA 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST JOINT INVENTOR: BERNHARD SCHÄTZLER

INVENTOR'S SIGNATURE: Bernhard Schätzler

DATE: 23.9.99

Residence: REGENSBURG, GERMANY

Country of Citizenship: GERMANY

Post Office Address: DR.-LEO-RITTER-STRASSE 59
D-93049 REGENSBURG
GERMANY

FULL NAME OF SECOND JOINT INVENTOR: GEORG ERNST

INVENTOR'S SIGNATURE: Georg Ernst

DATE: 23.9.99

Residence: THALMASSING, GERMANY

Country of Citizenship: GERMANY

Post Office Address: HAIDAUERSTRASSE 13
D-93107 THALMASSING
GERMANY
